PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of Michael A. Marra et al.	)	Group: 2121
Serial No.: 09/226,971	)	
Filed: January 8, 1999	)	
Title: METHOD OF REGULATING A TARGET SYSTEM USING A FREQUENCY COMPARISON OF FEEDBACK AND REFERENCE PULSE TRAINS	)	Examiner: S. R. Garland

BRIEF OF APPELLANT

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Commissioner for Patents
Washington, D.C. 20231

Sir:

This appeal is taken from the decision of the Examiner, dated July 26, 2001, finally rejecting claims 1-3, 5 and 8, and allowing claims 4, 6 and 7, which together are all of the claims that are under consideration in the above-captioned patent application. Appellants timely filed a Notice of Appeal relative to the rejection of claims 1-3, 5 and 8 on October 25, 2001.

I. REAL PARTY IN INTEREST

The real party in interest in this appeal is Lexmark International, Inc., a corporation organized and existing under the laws of the State of Delaware, which owns the entire interest in this patent application as set forth in the underlying claimed invention.

II. RELATED APPEALS AND INTERFERENCES

No related Appeals or Interferences are known to the Appellants.

III. STATUS OF CLAIMS

Pending: Claims 1 through 8.

Canceled: None.

Allowed: Claims 4, 6 and 7.

Objected To: None

Rejected: Claims 1 through 3, 5 and 8.

Withdrawn from Consideration: None.

On Appeal: Claims 1 through 3, 5 and 8.

IV. STATUS OF AMENDMENTS

No amendment was filed in this case subsequent to the final rejection. However, a Request for Reconsideration was filed on September 25, 2001. In an Advisory Action dated October 5, 2001, the Examiner indicated that the Request for Reconsideration did not place the application in condition for allowance.

V. SUMMARY OF INVENTION

The present invention relates generally to an automatic control system with feedback, and, more particularly, to proportional/integral/derivative (PID) automatic control systems using a feedback pulse train from a target system to be regulated. Schematically illustrated in Fig. 2, is an

embodiment of a PID control system using a feedback pulse train which may be used to carry out the method of the present invention. Target system 10 provides an output over line 12 in the form of a plurality of digital pulses, which define a feedback pulse train having a frequency. An example of such a pulse train is shown and labeled "encoder output" in Fig. 3. A digital PID control system 30 shown in Fig. 2 varies from PID control systems known in the art in that the feedback pulse train transmitted over line 12 is used directly in its outputted form to generate a control signal which is used to control target system 10. More particularly, a reference signal, such as a digital value, is provided over line 18. The digital reference signal is received by a converter 32 which converts the digital value of the signal to a plurality of digital pulses defining a reference pulse train having a frequency. The reference pulse train is provided as an output over line 34 to digital PID 36. The frequency of the reference pulse train received by digital PID 36 is compared with the frequency of the feedback pulse train received over line 12, rather than comparing digital values as is the case with conventional control systems. The comparison of the reference pulse train and the feedback pulse train results in the generation of a proportional error pulse train, which represents an error between the reference pulse train and the feedback pulse train. The proportional error pulse train is used to generate a proportional error term, integral error term, and derivatative error term, which in turn are used to generate a control signal which is outputted over line 38 to target system 10 to thereby control the operation of target system 10 (page 6, line 21, through page 8, line 2).

Fig. 3 shows, a graphical illustration of signal pulse trains generated and used by Appellants' invention, and the method of regulating target system 10 as shown in Fig. 2 is illustrated in further detail. A digital signal transmitted over line 18 in Fig. 2 is a value, which

corresponds to a desired reference pulse train (labeled "desired reference") with an associated constant frequency. The period of the desired reference pulse train is labeled Tref in Fig. 3. The desired reference pulse train is outputted from converter 32 to digital PID 36 (page 8, lines 3-10).

The feedback pulse train labeled "encoder output" is also received by digital PID 36 from target system 10. The feedback pulse train may have a constant or a varying frequency, dependent upon the operating state of target system 10. Digital PID 36 generates a reference pulse train (labeled "generated reference") having pulse widths which correspond to the width of a pulse of the signal labeled "desired reference" which is output from converter 32. Digital PID 36 aligns the leading edge of each pulse in the generated reference with the leading edge of each pulse in the feedback pulse train. The difference between each pair of aligned pulses is used to generate a proportional error pulse train (labeled "proportional error signal (P)") having a plurality of digital signals in the form of digital pulses. The width of each digital pulse in the proportional error signal corresponds to the difference between an aligned pair of pulses between the feedback pulse train and the generated reference. Based upon the comparison, the pulse of either the feedback pulse train or the generated reference having a greater width is used to generate an error direction pulse train (labeled "error direction signal (D)"). If the pulse width of the feedback pulse train is wider than the pulse width of the generated reference pulse train, the error direction signal transitions from a low state to a high state at the beginning of a pulse in the proportional error signal pulse train. On the other hand, if the pulse width of a pulse in the generated reference pulse train is wider than the pulse width of a corresponding pulse in the feedback pulse train, the error direction signal transitions from a high state to a low state at the leading edge of a corresponding pulse within the proportional error pulse train. Thus, the magnitude of an error is indicated by the

proportional error signal, and the directionality of the error is indicated by the error direction signal (page 8, line 11, through page 9, line 17).

Digital PID 36 may be in the form of a computer, or more preferably in the form of hard-wired circuitry used to make the frequency-to-frequency comparison described above between the feedback pulse train and desired reference pulse train. Digital PID 36 also includes timer circuitry which is used to carry out timing between transitions from a high state to a low state, and vice versa, of the proportional error pulse train and error direction pulse train described above. The timing circuitry allows the various timings to be carried out at a frequency which may be varied (page 9, line 18, through page 10, line 1).

Fig. 4 is a schematic illustration of an embodiment of a printer 40 which may be used to carry out the method of the present invention. Printer 40 is connected with a host 42 via a suitable electrical connection 43, such as a data bus, etc. Printer 40 includes an electrical processing circuit 44 which is used to control various portions of the operation of printer 40. For example, electrical processing circuit 44 is connected with a motor 46 which rotatably drives a roll 48. A sensor 50, such as an optical encoder, senses the passing of a plurality of markers 52 on roll 48, and provides a plurality of output signals in the form of a feedback pulse train which is transmitted via line 54 to electrical processing circuit 44. Thus, motor 46, roll 48 and sensor 50 may correspond to target system 10 shown in Fig. 2 (page 12, lines 8-21).

VI. ISSUES

1. Whether Claims 1 and 8 are anticipated under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,212,434 (Hsieh).

2. Whether Claims 2, 3 and 5 are unpatentable under 35 U.S.C. § 103(a) as being obvious over Hsieh in view of either U.S. Patent No. 4,494,509 (Long) or U.S. Patent No. 6,043,695 (O'Sullivan).

VII. GROUPING OF CLAIMS

Appellants submit that Claims 1 and 8 stand or fall together and claims 2, 3 and 5 stand or fall together.

VIII. ARGUMENT

1. CLAIMS 1 and 8 ARE PATENTABLE UNDER 35 U.S.C. § 102(b).

In the Final Office Action dated July 26, 2001, Claims 1 and 8 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,212,434 (Hsieh). However, Appellants submit that Claims 1 and 8 are neither taught, disclosed nor suggested by the cited references and are therefore in condition for allowance.

Hsieh discloses a phase-locked step motor speed servo controller, including motor 50, speed detector 60 and phase detector 10 (column 3, lines 27-47). Phase detector 10 has a first input port V, a second input port R, an output $V_1(t)$ and a phase error output θ_e. First input port V is connected to the output of speed detector 60 to receive feedback signal $P_1(t)$ having phase θ_1 and second input port R is connected to reference signal $P_2(t)$ whose phase is θ_2. The difference between the phase θ_1 of feedback signal $P_1(t)$ and phase θ_2 of reference signal $P_2(t)$ is the phase error θ_e ($\theta_e = \theta_1 - \theta_2$) (Fig.1 and column 3, line 47, through column 4, line 18). Phase error θ_e will cause up-down counter 22 to increase or decrease proportional to $\theta_e / 2\pi$, the count of which is

utilized to alter output voltage V_o, which is proportional to θ_e as shown in Fig. 5 (column 5, lines 27-44). V_o increases if θ_e indicates a phase lag, causing an increase in the rate of pulses sent to motor 50 in order to increase the speed of motor 50. Conversely, V_o decreases if θ_e indicates a phase lead, causing a decrease in the rate of pulses sent to motor 50 in order to decrease the speed of motor 50 (column 5, lines 46-63).

In contrast, claim 1 recites in part:

> generating a plurality of digital signals defining a reference pulse train with a frequency dependent upon said reference signal;
>
> providing a target system to be regulated, said target system having an output in the form of a plurality of digital signals defining a feedback pulse train having a frequency;
>
> comparing said frequency of said reference pulse train with said frequency of said feedback pulse train;
>
> generating a control signal based upon said comparison.

(Emphasis added) Appellants submit that such an invention is not taught, disclosed nor suggested by the cited references, alone or in combination, and includes distinct advantages thereover.

Hsieh compares the phase of a reference signal $P_2(t)$ to the phase of a feedback signal $P_1(t)$, and uses the difference thereof to create a phase error signal θ_e. Hsieh strives to reduce phase error signal θ_e by altering the driving signal to motor 50, thereby altering the speed of motor 50. Phase error θ_e causes up-down counter 22 to increase or decrease, depending on whether the phase error θ_e is positive or negative. The output of up-down counter 22 is converted to an analog signal, referred to as a pump voltage, which is used to increase or decrease the rate at which pulses are sent to motor 50. The change in the speed of motor 50 alters phase θ_1 of feedback signal $P_1(t)$. This change in phase θ_1 relative to phase θ_2 of reference signal $P_2(t)$ is continuously monitored and

sampled to control the speed of motor 50. Hsieh fails to disclose or suggest generating a reference pulse train, comparing the frequency of the reference pulse train with the frequency of a feedback pulse train and generating a control signal based upon the comparison, as recited in claim 1.

In the Final Rejection dated July 26, 2001, the Examiner implies that, elements 10, 30, 31, 60, 82 and the legends corresponding to Fig. 1 of Hsieh support the position that Hsieh anticipates the Appellants' invention. From the disclosure we find that element 10 is a phase detector, element 30 is a voltage-controlled pulse generator, element 31 is a divide-by-N_1 frequency divider, element 60 is a speed detector and element 82 is a divide-by-N_2 frequency divider. Appellants' invention has a converter 32 which receives a digital reference signal on line 18 and converts the digital value of the signal to a reference pulse train. However, this is distinct from Hsieh's voltage-controlled pulse generator 30 which receives an analog signal from D/A converter 23 and creates a pulse train to drive step motor 50, in that, the output of Appellants' converter 32 is a reference for comparing the frequency of a feedback pulse train received on line 12. In further contrast to Hsieh's phase comparison, Appellants' invention, as recited in claim 1, compares the frequencies of a reference signal and a feedback signal in Digital PID 36. Appellants' invention, as recited in claim 1, generates a reference pulse train, compares the frequency of the reference pulse train with the frequency of a feedback pulse train and generates a control signal based upon the comparison, which is not disclosed, taught or suggested in Hsieh by itself or in combination with any other cited reference.

The Examiner contends that 10 serves to compare pulse trains. However, phase detector 10 serves to <u>compare the phases</u> of two input signals.

The Hsieh disclosure, starting at column 4, line 12, recites in part:

> The phase detector 10 is capable of comparing ... the difference between the phase θ_1 of the feedback signal $P_1(t)$ and the phase θ_2 of the reference signal $P_2(t)$ and generating thereby a square pulse ... in proportion to the phase error θ_e.

(Emphasis Added). Whereas the Appellants' invention is not concerned with the phase of two signals, rather Appellants' invention, as recited in claim 1, compares the frequency of two signals. Herein lies a major advantage of Appellants' approach to speed control of a target, in that the complexity of phase comparison of two signals is obviated and the cost thereof eliminated. Hsieh measures phase differences of two signals and controls the speed of a target system to minimize the phase differences thereof. In contrast, Appellants' invention as recited in claim 1 compares the frequency of two signals and minimizes the frequency difference thereof. Appellants' invention, as recited in claim 1, has features not disclosed in the cited references, in that Appellants' invention generates a reference pulse train, compares the frequency of the reference pulse train with the frequency of a feedback pulse train and generates a control signal based upon the comparison, which is not disclosed, taught or suggested in Hsieh by itself or in combination with any other cited reference.

In summary, Hsieh does not teach, disclose or suggest generating a plurality of digital signals defining a reference pulse train with a frequency dependent upon said reference signal, and comparing the frequency of the reference pulse train with the frequency of the feedback pulse train, as recited, in part, in claim 1.

The present invention, as recited in claim 1, includes distinct advantages over Hsieh. One advantage of the Appellants' invention is that less space is needed for the frequency comparison circuitry than the phase detection circuitry of the references, since comparison of the relative

phases of two signals and the generation of a phase error correction signal are not necessary, as they are in the cited references. Another advantage of the Appellants' invention is that phase differences are not detected and not corrected; as a result thereof the circuitry of Appellants' invention has a reduced cost of implementation. Whereas, Appellants' invention is more economically implemented than a phase error detection method, the use of Appellants' invention will find broad appeal in design scenarios, where the controlling of a target by detecting phases of signals is cost prohibitive. Yet another advantage of Appellants' invention is that there is less electrical noise in the control system than is present in phase detection and control circuits.

For all of the foregoing reasons, Appellants submit that claim 1, and claim 8 depending therefrom, are in condition for allowance, the allowance of which is hereby respectfully requested.

2. CLAIMS 2, 3 and 5 ARE PATENTABLE UNDER 35 U.S.C. § 103(a).

In the Final Office Action dated July 26, 2001, Claims 2, 3 and 5 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,212,434 (Hsieh) in view of either U.S. Patent No. 4,494,509 (Long) or U.S. Patent No. 6,043,695 (O'Sullivan). Claims 2, 3 and 5 depend from claim 1, which is in condition for allowance for the reasons given above. Accordingly, claims 2, 3 and 5 are in condition for allowance because of their dependency from claim 1. Moreover claims 3 and 5 depend from claim 2, which, with the incorporation of the limitations of claim 1, is separately patentable and serves as the claim argued in this portion of the appeal.

Hsieh discloses a phase-locked step motor speed servo controller, including motor 50, speed detector 60 and phase detector 10 (column 3, lines 27-47). Phase detector 10 has a first

input port V, a second input port R, an output $V_1(t)$ and a phase error output θ_e. First input port V is connected to the output of speed detector 60 to receive feedback signal $P_1(t)$ having phase θ_1 and second input port R is connected to reference signal $P_2(t)$ whose phase is θ_2. The difference between the phase θ_1 of feedback signal $P_1(t)$ and phase θ_2 of reference signal $P_2(t)$ is the phase error θ_e ($\theta_e = \theta_1 - \theta_2$) (Fig.1 and column 3, line 47, through column 4, line 18). Phase error θ_e will cause up-down counter 22 to increase or decrease proportional to $\theta_e / 2\pi$, the count of which is utilized to alter output voltage V_o, which is proportional to θ_e as shown in Fig. 5 (column 5, lines 27-44). V_o increases if θ_e indicates a phase lag, causing an increase in the rate of pulses sent to motor 50 in order to increase the speed of motor 50. Conversely, V_o decreases if θ_e indicates a phase lead, causing a decrease in the rate of pulses sent to motor 50 in order to decrease the speed of motor 50 (column 5, lines 46-63).

Long discloses a high resolution electronic ignition control system including a Phase Locked Loop (PLL) 22 having a digital phase comparator 24. Phase comparator 24 develops an error signal fe as a sequence of pulses of a width proportional to the difference in phase of the leading edge of an incoming pulse X8PP is to the leading edge of an output pulse fvco (column 10, lines 58-65).

O'Sullivan discloses a PLL using a Schmitt trigger block including a phase comparator 21 which makes phase comparisons only on the rising edges of an input reference signal and a feedback signal (column 4, lines 59-65).

In contrast, claim 2 (incorporating the limitations of base claim 1) recites in part:

> generating a plurality of digital signals defining a reference pulse train with a frequency dependent upon said reference signal;

> providing a target system to be regulated, said target system having an output in the form of a plurality of digital signals defining a feedback pulse train having a frequency;
>
> comparing said frequency of said reference pulse train with said frequency of said feedback pulse train; ... and
>
> substantially aligning a leading edge of each digital signal in said reference pulse train with a leading edge of each digital signal in said feedback pulse train.

(Emphasis added) Appellants submit that such an invention is not taught, disclosed nor suggested by the cited references, alone or in combination, and includes distinct advantages thereover.

At page 3 of the Final Office Action dated July 26, 2001, the Examiner states that Hsieh does not disclose that the leading edges of pulses are used by a phase comparator to determine an error but that Long and O'Sullivan teach the comparing of leading edges of pulse trains for determining a phase error. Appellants agree with the Examiner that each of the three cited references teach the determination of a phase error between signals and that Long and O'Sullivan specifically teach the use of the leading edges of two signals to determine a phase error. However, Appellants invention does not compare leading edges of pulse trains, nor does it determine a phase error. In contrast to the cited references, Appellants invention, as recited in claim 2, aligns the leading edge of a reference pulse with a leading edge of a feedback pulse and no comparison or measurement of the differences in leading edge timing is undertaken. Whereas, Appellants invention intentionally aligns the leading edges of reference pulses, with the leading edges of feedback pulses, if such a limitation were a part of Hsieh, Long and/or O'Sullivan it would render their phase error detection non-functional since there would be no phase error to

detect between the leading edges of the two signals. None of the cited references, alone or in combination, teaches, discloses or suggests generating a plurality of digital signals defining a reference pulse train with a frequency dependent upon said reference signal, ... comparing the frequency of the reference pulse train with the frequency of the feedback pulse train and ... substantially aligning a leading edge of each digital signal in the reference pulse train with a leading edge of each digital signal in the feedback pulse train, as recited, in part, in claim 2.

Appellants' invention, as recited in claim 2, includes distinct advantages over the cited references. One advantage of the Appellants' invention is that less space is needed for the frequency comparison circuitry than the phase detection circuitry of the references, since comparison of the relative phases of two signals and the generation of a phase error correction signal are not necessary, as they are in the cited references. Another advantage of the Appellants' invention is that phase differences are not detected and not corrected; as a result thereof the circuitry of Appellants' invention has a reduced cost of implementation. Whereas, Appellants' invention is more economically implemented than a phase error detection method, the use of Appellants' invention will find broad appeal in design scenarios, where the controlling of a target by detecting phases of signals is cost prohibitive. Yet another advantage of Appellants' invention is that there is less electrical noise in the control system than is present in phase detection and control circuits.

For all of the foregoing reasons, Appellants submit that claim 2, and claims 3 and 5 depending therefrom, are in condition for allowance, the allowance of which is hereby respectfully requested.

IX. CONCLUSION

For the foregoing reasons, Appellant submits that claims 1-3, 5 and 8 are neither anticipated nor suggested by the cited references, alone or in combination, and are therefore in condition for allowance in their present form. Accordingly, Appellants respectfully request the Board to reverse the final rejections of the appealed claims.

Respectfully submitted,

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Date

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X. APPENDIX

1. A method of regulating a target system, comprising the steps of:

providing a reference signal;

generating a plurality of digital signals defining a reference pulse train with a frequency dependent upon said reference signal;

providing a target system to be regulated, said target system having an output in the form of a plurality of digital signals defining a feedback pulse train having a frequency;

comparing said frequency of said reference pulse train with said frequency of said feedback pulse train;

generating a control signal dependent upon said comparison; and

providing said control signal as an input to said target system.

2. The method of regulating a target system of claim 1, wherein said comparing step comprises substantially aligning a leading edge of each digital signal in said reference pulse train with a leading edge of each digital signal in said feedback pulse train.

3. The method of regulating a target system of claim 2, wherein said step of generating said control signal comprises the substep of generating a proportional error pulse train including a plurality of digital signals, each said digital signal representing an error between a corresponding pair of aligned digital signals of said reference pulse train and said feedback pulse train.

4. A method of regulating a target system, comprising the steps of:

providing a reference signal;

generating a plurality of digital signals defining a reference pulse train with a frequency dependent upon said reference signal;

providing a target system to be regulated, said target system having an output in the form of a plurality of digital signals defining a feedback pulse train having a frequency;

comparing said frequency of said reference pulse train with said frequency of said feedback pulse train;

substantially aligning a leading edge of each digital signal in said reference pulse train with a leading edge of each digital signal in said feedback pulse train;

generating a control signal dependent upon said comparison, said generating step including the substeps of:

generating a proportional error pulse train including a plurality of digital signals, each said digital signal representing an error between a corresponding pair of aligned digital signals of said reference pulse train and said feedback pulse train;

counting up from zero with a first proportional clock CP1 at a frequency fP1 when said digital signals of said proportional error pulse train are in a high state;

resetting said first proportional clock CP1 to zero when said digital signals of said proportional error pulse train are in a low state;

loading a current value of said first proportional clock CP1 into a second proportional clock CP2 each time said first proportional clock CP1 transitions from

a high state to a low state;

counting down from said loaded current value with said second proportional clock CP2 at a frequency fP2 until a zero value is reached; and

determining a proportional error term representing a time average of a signal which is held high while said second proportional clock CP2 is in a high state and held low while said second proportional clock CP2 is in a zero state, said control signal being dependent upon said proportional error term; and

providing said control signal as an input to said target system.

5. The method of regulating a target system of claim 3, wherein said step of generating said control signal comprises the further substep of generating an error direction pulse train including a plurality of digital signals, each said digital signal representing a directionality of said error between said corresponding pair of aligned digital signals.

6. A method of regulating a target system, comprising the steps of:

providing a reference signal;

generating a plurality of digital signals defining a reference pulse train with a frequency dependent upon said reference signal;

providing a target system to be regulated, said target system having an output in the form of a plurality of digital signals defining a feedback pulse train having a frequency;

comparing said frequency of said reference pulse train with said frequency of said feedback pulse train, and substantially aligning a leading edge of each digital signal in said reference pulse

train with a leading edge of each digital signal in said feedback pulse train;

generating a control signal dependent upon said comparison, said generating step including the substeps of:

generating a proportional error pulse train including a plurality of digital signals, each said digital signal representing an error between a corresponding pair of aligned digital signals of said reference pulse train and said feedback pulse train;

generating an error direction pulse train including a plurality of digital signals, each said digital signal representing a directionality of said error between said corresponding pair of aligned digital signals;

counting up from zero with a first integral clock CI1 at a frequency fI1 when said digital signals of said proportional error pulse train are in a high state and said digital signals of said error direction pulse train are simultaneously in a high state;

counting down with said first integral clock CI1 at said frequency fI1 when said digital signals of said proportional error pulse train are in a high state and said digital signals of said error direction pulse train are in a low state;

maintaining said first integral clock CI1 at a current value when said digital signals of said proportional error pulse train are in a low state;

loading a current value of said first integral clock CI1 into a second integral clock CI2 each time said first integral clock CI1 transitions from a high state to a low state;

counting down from said loaded current value with said second integral

clock CI2 at a frequency fI2 until a zero value is reached; and

determining an integral error term representing a time average of a signal which is held high while said second integral clock CI2 is in a high state and held low while said second integral clock CI2 is in a zero state, said control signal being dependent upon said integral error term; and

providing said control signal as an input to said target system.

7. A method of regulating a target system, comprising the steps of:

providing a reference signal;

generating a plurality of digital signals defining a reference pulse train with a frequency dependent upon said reference signal;

providing a target system to be regulated, said target system having an output in the form of a plurality of digital signals defining a feedback pulse train having a frequency;

comparing said frequency of said reference pulse train with said frequency of said feedback pulse train, and substantially aligning a leading edge of each digital signal in said reference pulse train with a leading edge of each digital signal in said feedback pulse train;

generating a control signal dependent upon said comparison, said generating step including the substeps of:

generating a proportional error pulse train including a plurality of digital signals, each said digital signal representing an error between a corresponding pair of aligned digital signals of said reference pulse train and said feedback pulse train;

counting up from zero with a first derivative clock CD1 at a frequency fD1

when said digital signals of said proportional error pulse train are in a high state;

subtracting a current state of said first derivative clock CD1 from a current state of a register R each time said first derivative clock CD1 transitions from a high state to a low state;

loading said subtracted state into a second derivative clock CD2;

loading said current state of said first derivative clock CD1 into said register R;

resetting said first derivative clock CD1 to zero;

counting down with said second derivative clock CD2 at a frequency fD2 after said subtracted state is loaded therein;

maintaining said first integral clock CI1 at a current value when said digital signals of said proportional error pulse train are in a low state; and

determining a derivative error term representing a time average of a signal which is held high while said second derivative clock CD2 is in a high state and held low while said second derivative clock CD2 is in a zero state, said control signal being dependent upon said derivative error term; and

providing said control signal as an input to said target system.

8. The method of regulating a target system of claim 1, wherein said frequency of said feedback pulse train varies with time.